M500DC 2.5-Inch SATA NAND Flash SSD

MTFDDAK120MBB-1AE1ZABYY, MTFDDAK240MBB-1AE1ZABYY, MTFDDAK480MBB-1AE1ZABYY, MTFDDAK800MBB-1AE1ZABYY

Features

- Micron® 20nm MLC NAND Flash
- RoHS-compliant package
- SATA 6 Gb/s interface
- ATA modes supported
  - PIO mode 3, 4
  - Multiword DMA mode 0, 1, 2
  - Ultra DMA mode 0, 1, 2, 3, 4, 5
- Enterprise sector size support
  - 512-byte
- Hot-plug capable
- Native command queuing support with 32-command slot support
- ATA-8 ACS2 command set compliant
- ATA security feature command set and password login support
- Security erase command set: fast and secure erase
- Self-monitoring, analysis, and reporting technology (SMART) command set
- 120GB performance (steady state) [1, 2]
  - Sequential 128KB read: 425 MB/s
  - Sequential 128KB write: 200 MB/s
  - Random 4KB read: 63,000 IOPS
  - Random 4KB write: 23,000 IOPS
  - READ latency: 0.50ms
  - WRITE latency: 1.5ms
- 240GB performance (steady state) [1, 2]
  - Sequential 128KB read: 425 MB/s
  - Sequential 128KB write: 330 MB/s
  - Random 4KB read: 63,000 IOPS
  - Random 4KB write: 33,000 IOPS
  - READ latency: 0.50ms
  - WRITE latency: 1.5ms
- 480GB performance (steady state) [1, 2]
  - Sequential 128KB read: 425 MB/s
  - Sequential 128KB write: 375 MB/s
  - Random 4KB read: 63,000 IOPS
  - Random 4KB write: 35,000 IOPS
  - READ latency: 0.50ms
  - WRITE latency: 1.5ms
- 800GB performance (steady state) [1, 2]
  - Sequential 128KB read: 425 MB/s
  - Sequential 128KB write: 375 MB/s
  - Random 4KB read: 65,000 IOPS
  - Random 4KB write: 24,000 IOPS
  - READ latency: 0.50ms
  - WRITE latency: 1.5ms
- Reliability
  - Mean time to failure (MTTF): 2 million device hours[3]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{16} bits read
  - End-to-end data protection
  - Enhanced power-loss data protection with data protection capacitor monitoring
- Endurance: Total bytes written (TBW)
  - 120GB: 0.5PB; 240GB: 1.0PB; 480GB: 1.9PB; 800GB: 1.9PB
- Capacity[4] (unformatted): 120GB, 240GB, 480GB, 800GB
- Mechanical: 7.0mm height
  - SATA connector: 5V ±10%
  - 2.5-inch drive: 100.2mm x 69.85mm x 7.0mm
  - Conforms to SFF standards
- Field-upgradeable firmware
- Power consumption: <6.0W (TYP); <6.3W (TYP) for 800GB
- Operating temperature
  - Commercial (0°C to 70°C)[5]

Notes:
1. Typical I/O performance numbers as measured using Iometer with a queue depth of 32 and write cache disabled.
2. 4KB transfers used for READ/WRITE latency values.
3. The product achieves a MTTF based on population statistics not relevant to individual units.
4. 1GB = 1 billion bytes; formatted capacity is less.
5. Drive case temperature.

Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

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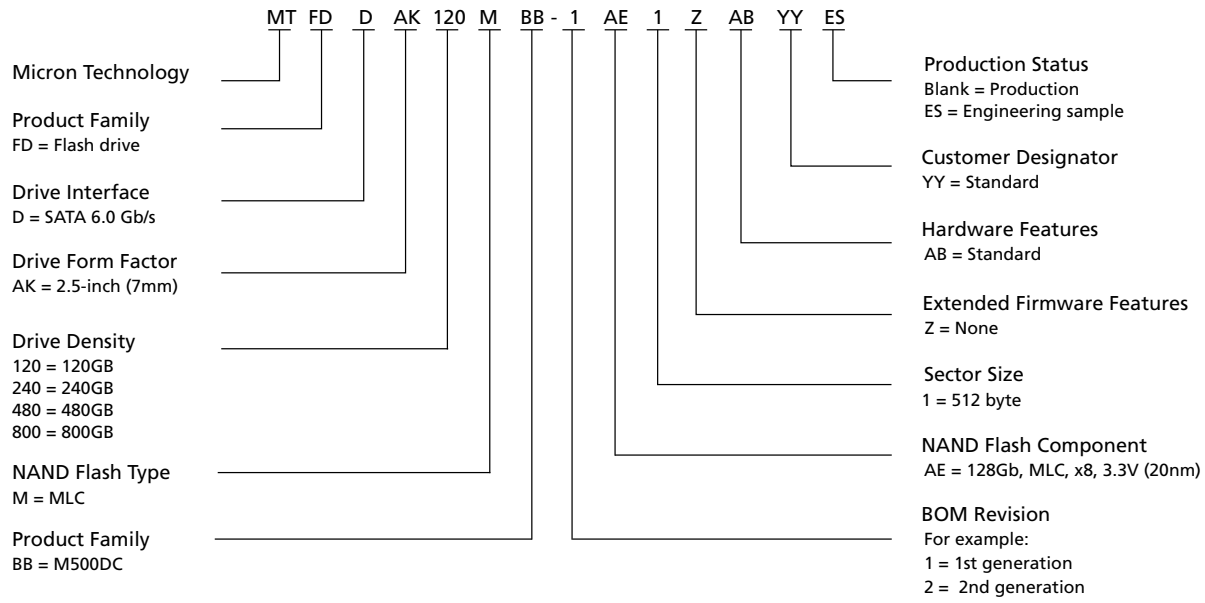
Part Numbering Information

Micron's M500DC SSD is available in different configurations and densities. Visit micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



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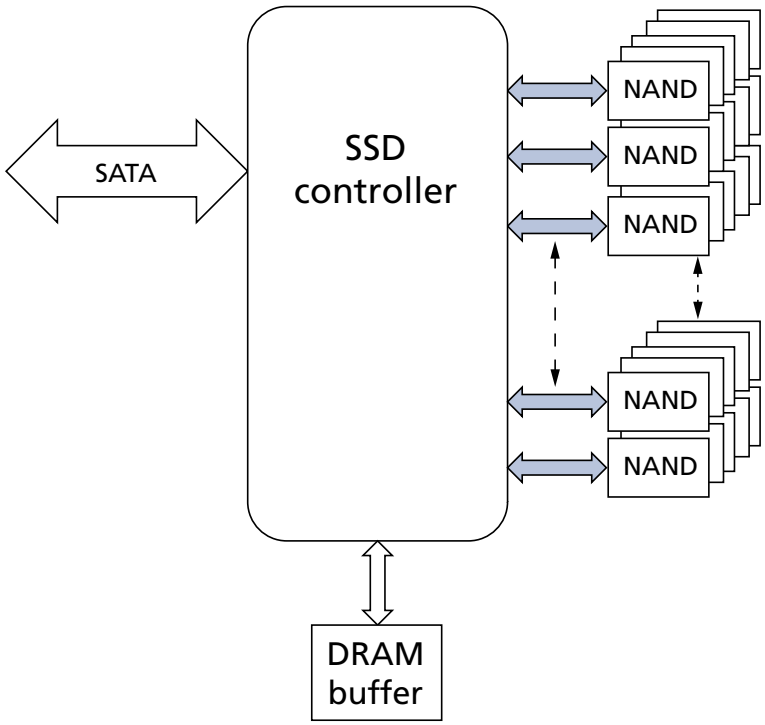
General Description

Micron's M500DC solid state drive (SSD) uses a single-chip controller with a SATA interface on the system side and n-channels of Micron NAND Flash internally. Packaged in an HDD replacement enclosure, the SSD integrates easily in existing storage infrastructures.

The M500 DC is designed to support and manage the needs of enterprise platforms that utilize high IOPs traffic previously supported solely by SLC solutions, it provides the performance, endurance, and data integrity required by these growing environments.

Figure 2: Functional Block Diagram



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Logical Block Address Configuration

The drive is set to report the number of logical block addresses (LBA) that will ensure sufficient storage space for the specified density. Standard LBA settings, based on the IDEMA standard (LBA1-02), are shown below.

Table 1: Standard LBA Settings – 512-Byte Sector Size

Drive Size	Total LBA		Max LBA		User Available Bytes
	Decimal	Hexadecimal	Decimal	Hexadecimal	(Unformatted)
120GB	234,441,648	DF94BB0	234,441,647	DF94BAF	120,034,123,776
240GB	468,862,128	1BF244B0	468,862,127	1BF244AF	240,057,409,536
480GB	937,703,088	37E436B0	937,703,087	37E436AF	480,103,981,056
800GB	1,562,824,368	5D26CEB0	1,562,824,367	5D26CEAF	800,166,076,416

Physical Configuration

Table 2: 2.5-Inch Dimensions

Specification	Value		Unit
	Nom	Max	
Height	–	7.0	mm
Width	69.85	–	mm
Length	100.20	–	mm

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Interface Connectors

The SATA signal segment interface cable has four conductors and three ground connections. As shown in Package Dimensions, the cable includes a 7-pin signal segment and a 15-pin power segment arranged in a single row with a 1.27mm (0.050in) pitch.

Table 3: SATA Signal Segment Pin Assignments

Signal Name	Type	Description
S1	GND	Ground
S2	A	Differential signal pair A and A#
S3	A#	
S4	GND	Ground
S5	B#	Differential signal pair B and B#
S6	B	
S7	GND	Ground

Table 4: 2.5-Inch SATA Power Segment Pin Assignments

Pin#	Signal Name	Description
P1	V33	No connect
P2	V33	No connect
P3	V33	No connect
P4	GND	Ground
P5	GND	Ground
P6	GND	Ground
P7	V5	5V power, precharge
P8	V5	5V power
P9	V5	5V power
P10	GND	Ground
P11	DAS	Device activity signal
P12	GND	Ground
P13	V12	No connect
P14	V12	No connect
P15	V12	No connect

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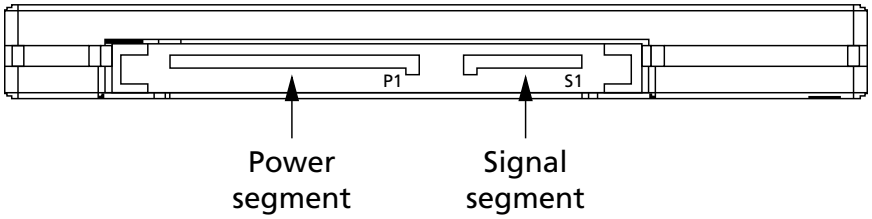
Figure 3: SSD Interface Connections



Device ID

Table 5: Identify Device

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
0	–	–	–	General configuration bit-significant information
	15	F	0b	0 = ATA device
	14–8	X	0000100	Retired
	7	F	0b	1 = Removable media device
	6	F	1b	Obsolete
	5–3	X	000b	Retired
	2	V	0b	Response incomplete
	1	X	0b	Retired
	0	F	0b	Reserved
1	–	–	3FFFh	Obsolete
2	–	F	C837h	Specific configuration
3	–	F	0010h	Obsolete
4	–	F	0000h 0000h	Retired
6	–	F	003Fh	Obsolete
7	–	(O)V	0000h 0000h	Reserved for assignment by the CompactFlash™ Association
9	–	( )X	0000h	Retired
10	–	(M)F	Varies	Serial number (20 ASCII characters)
20	–	( )X	0000h 0000h 0000h	Retired/obsolete
23	–	(M)F	Varies	Firmware revision (8 ASCII characters)
27	–	(M)F	Varies	Model number (40 ASCII characters)
47	15–8	F	80h	80h
	7–0	F	10h	00h = Reserved 01h-FFh = Maximum number of logical sectors that shall be transferred per DRQ data block on READ/WRITE MULTIPLE commands

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
48	–	–	–	Trusted Computing feature set options
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–1	F	0000000000000b	Reserved for the Trusted Computing Group
	0	F	0b	1 = Trusted Computing feature set is supported
49	–	–	–	Capabilities
	15–14	F	00b	Reserved for the IDENTIFY PACKET DEVICE command
	13	F	1b	1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device
	12	F	0b	Reserved for the IDENTIFY PACKET DEVICE command
	11	F	1b	1 = IORDY is supported 0 = IORDY may be supported
	10	F	1b	1 = IORDY may be disabled
	9	–	1b	1 = LBA is supported
	8	F	1b	1 = DMA is supported
	7–0	F	00000000b	Retired
50	–	–	–	Capabilities
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–2	F	000000000000b	Reserved
	1	X	0b	Obsolete
	0	F	1b	Shall be set to one to indicate a vendor-specific standby timer value minimum
51	–	( )X	0000h 0000h	Obsolete
53	15–3	F	0000000000000b	Reserved
	2	F	1b	1 = The fields reported in word 88 are valid 0 = The fields reported in word 88 are not valid
	1	F	1b	1 = The fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid
	0	X	1b	Obsolete
54	–	( )X	3FFFh 0010h 003Fh FC10h 00FBh	Obsolete

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
59	15	F	1b	1 = The BLOCK ERASE EXT command is supported
	14	F	1b	1 = The OVERWRITE EXT command is supported
	13	F	1b	1 = The CRYPTO SCRAMBLE EXT command is supported
	12	F	1b	1 = The sanitize feature set is supported
	11–9	F	000b	Reserved
	8	V	1b	1 = Multiple sector settings are valid
	7–0	V	00010000b	xxh = Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE MULTIPLE commands
60	–	M(F)	Varies by capacity	Total number of user addressable logical sectors
62	–	( )X	0000h	Obsolete
63	15–11	F	00000b	Reserved
	10	V	0b	1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected
	9	V	0b	1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected
	8	V	0b	1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected
	7–3	F	0000b	Reserved
	2	F	1b	1 = Multiword DMA mode 2 and below are supported
	1	F	1b	1 = Multiword DMA mode 1 and below are supported
	0	F	1b	1 = Multiword DMA mode 0 is supported
64	15–8	F	00h	Reserved
	7–0	F	03h	PIO modes is supported
65	–	F	0078h	Minimum Multiword DMA transfer cycle time per word Cycle time in nanoseconds
66	–	F	0078h	Manufacturer's recommended Multiword DMA transfer cycle time Cycle time in nanoseconds
67	–	F	0078h	Minimum PIO transfer cycle time without flow control Cycle time in nanoseconds
68	–	F	0078h	Minimum PIO transfer cycle time with IORDY flow control Cycle time in nanoseconds

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
69	–	F	–	Additional supported
	15	F	0b	1 = CFast specification is supported
	14	F	1b	1 = Deterministic read after trim is supported
	13	F	0b	1 = Long physical sector alignment error reporting control is supported
	12	F	0b	1 = DEVICE CONFIGURATION IDENTIFY DMA and DEVICE CONFIGURATION SET DMA are supported
	11	F	0b	1 = READ BUFFER DMA is supported
	10	F	0b	1 = WRITE BUFFER DMA is supported
	9	F	1b	1 = SET MAX PASSWORD DMA and SET MAX UNLOCK DMA are supported
	8	F	0b	1 = DOWNLOAD MICROCODE DMA is supported
	7	F	0b	Reserved for IEEE-1667
	6	F	0b	1 = Optional ATA device 28-bit commands are supported
	5	F	1b	1 = Read zero after trim is supported
	4	F	0b	1 = Device encrypts all user data (per ATA8-ACS2)
	3	F	0b	1 = Extended number of user addressable sectors is supported (words 230 – 233)
	2–0	F	000b	Reserved
70	–	F	0000h	Reserved
71	–	F	0000h 0000h 0000h 0000h	Reserved for the IDENTIFY PACKET DEVICE command
75	–	–	–	Queue depth
	15–5	F	00000000000b	Reserved
	4–0	F	11111b	Maximum queue depth - 1

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
76	–	–	–	Serial ATA capabilities
	15	F	1b	1 = Supports READ LOG DMA EXT as equivalent to READ LOG EXT
	14	F	0b	1 = Supports Device automatic partial to slumber transitions
	13	F	0b	1 = Supports host automatic partial to slumber transitions
	12	F	1b	Native command queuing priority information is supported
	11	F	0b	Unload while NCQ commands are outstanding is supported
	10	F	1b	Physical event counters are supported
	9	F	0b	1 = Receipt of host-initiated interface power management requests is supported
	8	F	1b	Native command queuing is supported
	7–4	F	0000b	Reserved for future Serial ATA signaling speed grades
	3	F	1b	1 = Serial ATA Gen-3 speed (6.0 Gb/s) is supported
	2	F	1b	1 = Serial ATA Gen-2 speed (3.0 Gb/s) is supported
	1	F	1b	1 = Serial ATA Gen-1 speed (1.5 Gb/s) is supported
	0	F	0b	Reserved (set to 0)
77	–	–	–	Serial ATA additional capabilities
	15–7	F	000000000b	Reserved for future Serial ATA definition
	6	F	1b	1 = Supports RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED commands
	5	F	0b	NCQ QUEUE MANAGEMENT command is supported
	4	F	0b	NCQ streaming is supported
	3–1	V	011b	Coded value indicating current negotiated Serial ATA signal speed
	0	F	0b	Shall be cleared to zero
78	–	–	–	Serial ATA features are supported
	15–7	F	000000000b	Reserved
	6	F	1b	1 = Supports software settings preservation
	5	F	0b	Reserved
	4	F	0b	1 = In-order data delivery is supported
	3	F	0b	1 = Dev initiate interface power management is supported
	2	F	1b	1 = DMA setup auto-activate optimization is supported
	1	F	0b	1 = Non-zero buffer offsets in DMA setup FIS are supported
	0	F	0b	Reserved (set to 0)

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
79	–	–	–	Serial ATA features are enabled
	15–7	V	000000000b	Reserved
	6	V	1b	1 = Software settings preservation is enabled
	5	V	0b	1 = Asynchronous notification is enabled
	4	V	0b	1 = In-order data delivery is enabled
	3	V	0b	1 = Device initiating interface power management is enabled
	2	V	0b	1 = DMA setup auto-activate optimization is enabled
	1	V	0b	1 = Non-zero buffer offsets in DMA setup FIS is enabled
	0	V	0b	Reserved (set to 0)
80	–	–	–	Major revision number
	15–10	F	000000b	Reserved
	9	F	1b	1 = ATA8-ACS2 is supported
	8	F	1b	1 = ATA8-ACS is supported
	7	F	1b	1 = ATA/ATAPI-7 is supported
	6	F	1b	1 = ATA/ATAPI-6 is supported
	5	F	1b	1 = ATA/ATAPI-5 is supported
	4	F	1b	1 = ATA/ATAPI-4 is supported
	3	F	1b	Obsolete
	2	S	0b	Obsolete
	1	S	0b	Obsolete
	0	F	0b	Reserved
81	–	F	0028h	Minor revision number

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
82	–	–	–	Command set is supported
	15	X	0b	Obsolete
	14	F	1b	1 = NOP command is supported
	13	F	1b	1 = READ BUFFER command is supported
	12	F	1b	1 = WRITE BUFFER command is supported
	11	X	0b	Obsolete
	10	F	1b	1 = Host-protected area feature set is supported
	9	F	0b	1 = DEVICE RESET command is supported
	8	F	0b	1 = Service interrupt is supported
	7	F	0b	1 = Release interrupt is supported
	6	F	1b	1 = Read look-ahead is supported
	5	F	1b	1 = Write cache is supported
	4	F	0b	Shall be cleared to zero to indicate that the packet feature set is not supported
	3	F	1b	1 = Mandatory power management feature set is supported
	2	F	0b	Obsolete
	1	F	1b	1 = Security feature set is supported
	0	F	1b	1 = SMART feature set is supported
83	–	–	–	Command set is supported
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = FLUSH CACHE EXT command is supported
	12	F	1b	1 = Mandatory FLUSH CACHE command is supported
	11	F	1b	1 = Device configuration overlay feature set is supported
	10	F	1b	1 = 48-bit address feature set is supported
	9	F	0b	1 = Automatic acoustic management feature set is supported
	8	F	1b	1 = SET MAX security extension is supported
	7	F	0b	See Address Offset Reserved Area Boot INCITS TR27:2001
	6	F	0b	1 = SET FEATURES subcommand required to spin-up after power-up
	5	F	0b	1 = Power-up in standby feature set is supported
	4	F	0b	Obsolete
	3	F	1b	1 = Advanced power management feature set is supported
	2	F	0b	1 = CFA feature set is supported
	1	F	0b	1 = READ/WRITE DMA QUEUED is supported
	0	F	1b	1 = DOWNLOAD MICROCODE command is supported

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
84	–	–	–	Command set/feature-supported extension
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = Idle immediate with unload feature is supported
	12	F	0b	Reserved for technical report INCITS TR-37-2004 (TLC)
	11	F	0b	Reserved for technical report INCITS TR-37-2004 (TLC)
	10–9	F	00b	Obsolete
	8	F	1b	1 = 64-bit word wide name is supported
	7	F	0b	1 = WRITE DMA QUEUED FUA EXT command is supported
	6	F	1b	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
	5	F	1b	1 = General purpose logging feature set is supported
	4	F	0b	1 = Streaming feature set is supported
	3	F	0b	1 = Media card pass through command feature set is supported
	2	F	0b	1 = Media serial number is supported
	1	F	1b	1 = SMART self-test is supported
	0	F	1b	1 = SMART error logging is supported
85	–	–	–	Command set/feature is enabled
	15	X	0b	Obsolete
	14	F	1b	1 = NOP command is supported
	13	F	1b	1 = READ BUFFER command is supported
	12	F	1b	1 = WRITE BUFFER command is supported
	11	X	0b	Obsolete
	10	V	1b	1 = Host protected area feature set is enabled
	9	F	0b	1 = DEVICE RESET command is supported
	8	V	0b	1 = SERVICE interrupt is enabled
	7	V	0b	1 = Release interrupt is enabled
	6	V	1b	1 = Look-ahead is enabled
	5	V	1b	1 = Write cache is enabled
	4	F	0b	Shall be cleared to zero to indicate that the packet feature set is not supported
	3	F	1b	Power management feature set is enabled
	2	F	0b	Obsolete
	1	V	0b	1 = Security mode feature set is enabled
	0	V	1b	1 = SMART feature set is enabled

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
86	–	–	–	Command set/feature is enabled
	15		1b	1 = Words 120-119 are valid
	14	F	0b	1 = Reserved
	13	F	1b	1 = FLUSH CACHE EXT command is supported
	12	F	1b	1 = FLUSH CACHE command is supported
	11	F	1b	1 = Device configuration overlay is supported
	10	F	1b	1 = 48-bit address feature set is supported
	9	V	0b	1 = Automatic acoustic management feature set is enabled
	8	F	0b	1 = SET MAX security enabled by SET MAX SET PASSWORD
	7	F	0b	Reserved for address offset reserved area boot, INCITS TR27:2001
	6	F	0b	1 = SET FEATURES subcommand required to spin-up after power-up
	5	V	0b	1 = Power-up in standby feature set is enabled
	4	V	0b	Obsolete
	3	V	1b	1 = Advanced power management feature set is enabled
	2	F	0b	1 = CFA feature set is supported
	1	F	0b	1 = READ/WRITE DMA QUEUED command is supported
	0	F	1b	1 = DOWNLOAD MICROCODE command is supported
87	–	–	–	Command set/feature is enabled/supported
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = IDLE IMMEDIATE with UNLOAD FEATURE is supported
	12	V	0b	Reserved for technical report- INCITS tr-37-2004 (TLC)
	11	V	0b	Reserved for technical report- INCITS TR-37-2004 (TLC)
	10–9	F	00b	Obsolete
	8	F	1b	1 = 64-bit word wide name is supported
	7	F	0b	1 = WRITE DMA QUEUED FUA EXT command is supported
	6	F	1b	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
	5	F	1b	1 = General purpose logging feature set is supported
	4	V	0b	Obsolete
	3	V	0b	1 = Media card pass through command feature set is supported
	2	V	0b	1 = Media serial number is valid
	1	F	1b	1 = SMART self-test is supported
	0	F	1b	1 = SMART error logging is supported

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
88	–	–	0b	Ultra DMA modes
	15	–	0b	Reserved
	14	–	0b	1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
	13	–	0b	1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
	12	–	0b	1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
	11	–	0b	1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
	10	–	0b	1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
	9	–	0b	1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
	8	–	0b	1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
	7	–	0b	Reserved
	6	–	1b	1 = Ultra DMA mode 6 and below are supported
	5	–	1b	1 = Ultra DMA mode 5 and below are supported
	4	–	1b	1 = Ultra DMA mode 4 and below are supported
	3	–	1b	1 = Ultra DMA mode 3 and below are supported
	2	–	1b	1 = Ultra DMA mode 2 and below are supported
	1	–	1b	1 = Ultra DMA mode 1 and below are supported
	0	–	1b	1 = Ultra DMA mode 0 is supported
89	–	(O)F	0001h	Time required for security erase unit completion
90	–	(O)F	0001h	Time required for enhanced security erase completion
91	–	(O)V	00FEh	Current advanced power management value
92	–	(O)V	FFFEh	Master password revision code

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
93	–	–	–	Shall be 0000h for SATA devices
	15	–	0b	Shall be cleared to zero
	14	–	0b	Shall be set to one
	13	–	0b	1 = Device detected CBLID-above V_{IH} 0 = device detected CBLID-below V_{IL}
	–	–	–	Device 1 hardware reset result Device 0 shall clear these bits to zero Device 1 shall set these bits in accordance with the ATA8, ACS2 specification. See specification for details.
	12	–	0b	Reserved
	11	–	0b	0 = Device 1 did not assert PDIAG- 1 = Device 1 asserted PDIAG-
	10–9	–	00b	These bits indicate how device 1 determined the device number: 00 = Reserved 01 = A jumper was used 10 = The CSEL signal was used 11 = Some other method was used or the method is unknown
	8	–	0b	Shall be set to one
		–		Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits in accordance with the ATA8, ACS2 specification. See specification for details.
	7	–	0b	Reserved
	6	–	0b	0 = Device 0 does not respond when device 1 is selected. 1 = Device 0 responds when device 1 is selected
	5	–	0b	0 = Device 0 did not detect the assertion of DASP- 1 = Device 0 detected the assertion of DASP-
	4	–	0b	0 = Device 0 did not detect the assertion of PDIAG- 1 = Device 0 detected the assertion of PDIAG-
	3	–	0b	0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics
	2–1	–	00b	These bits indicate how device 0 determined the device number: 00 = Reserved 01 = A jumper was used 10 = The CSEL signal was used 11 = Some other method was used or the method is unknown
	0	–	0b	Shall be set to one
94	15–8	F	00h	Vendor's recommended acoustic management value
	7–0	V	00h	Current automatic acoustic management value
95	–	(O)V	0000h	Stream minimum request size

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
96	–	(O)V	0000h	Streaming transfer time - DMA
97	–	(O)V	0000h	Streaming access latency - DMA and PIO
98	–	(O)F	0000h 0000h	Streaming performance granularity (98-99)
100	–	V	Varies by capacity	Maximum user LBA for 48-bit address feature set
104	–	(O)V	0000h	Streaming transfer time - PIO
105	–	( )F	0008h	Maximum number of 512-byte blocks of LBA range entries per DATA SET MANAGEMENT command
106	–	–	–	Physical sector size/logical sector size
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = Device has multiple logical sectors per physical sector
	12	F	0b	1 = Device logical sector longer than 256 Words
	11–4	F	00000000b	Reserved
	3–0	F	0011b	8 logical sectors per physical sector
107	–	(O)F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108	15–12	F	0101b	NAA (3-0)
	11–0	–	000000001010b	IEEE OUI (23-12)
109	15–4	F	000001110101b	IEEE OUI (11-0)
	3–0	–	Varies	Unique ID (35-32)
110	–	(M)F	Varies	5-0 unique ID (31-16)
111	–	(M)F	Varies	Unique ID (15-0)
112	–	(O)F	0000h 0000h 0000h 0000h	Reserved for 128-bit world wide name extension to 128 bits
116	–	(O)V	0000h	Reserved for INCITS TR-37-2004
117	–	(O)F	0000h 0000h	Words per logical sector

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
119	–	–	–	Commands and feature sets are supported (continued from words 84-82)
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–8	F	00000000b	Reserved
	7	F	0b	1 = Extended power conditions feature set is supported
	6	F	0b	1 = Extended status reporting feature set is supported
	5	F	0b	1 = Free-fall control feature set is supported
	4	F	1b	1 = DOWNLOAD MICROCODE command with mode 3 supported
	3	F	1b	1 = READ LOG DMA EXT and WRITE LOG DMA EXT commands supported
	2	F	1b	1 = Write uncorrectable EXT command is supported
	1	F	1b	1 = Write-read-verify feature set is supported
	0	F	0b	Reserved for DDT
120	–	–	–	Commands and feature sets are supported or enabled (continued from words 87-85)
	15	–	0b	Shall be cleared to zero
	14	–	1b	Shall be set to one
	13–6	–	00000000b	Reserved
	5	–	0b	1 = Free-fall control feature set is enabled
	4	–	1b	1 = The DOWNLOAD MICROCODE command with mode 3 is supported
	3	–	1b	1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
	2	–	1b	1 = The WRITE UNCORRECTABLE EXT command is supported
	1	–	0b	1 = The write-read-verify feature set is enabled
	0	–	0b	1 = The disable data transfer after error detection feature set is enabled 0 = The disable data transfer after error detection feature set is disabled
121	–	F	0000h 0000h 0000h 0000h 0000h 0000h	Reserved for expanded, supported, and enabled settings
127	–	(O)	0000h	Obsolete

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
128	–	–	–	Security status
	15–9	F	0000000b	Reserved
	8	V	0b	Security level 0 = High, 1 = Maximum
	7–6	F	00b	Reserved
	5	F	1b	1 = Enhanced security erase is supported
	4	V	0b	1 = Security count is expired
	3	V	0b	1 = Security is frozen
	2	V	0b	1 = Security is locked
	1	V	0b	1 = Security is enabled
	0	F	1b	1 = Security is supported
129	–	( )X	Vendor-specific data	Vendor specific
160	–	–	–	CFA power mode 1
	15	F	0b	Word 160 is supported
	14	F	0b	Reserved
	13	F	0b	CFA power mode 1 is required for one or more commands implemented by the device
	12	V	0b	CFA power mode 1 is disabled
	11–0	F	000000000000b	Maximum current in ma
161	–	X	0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved for assignment by the CompactFlash Association
168	15–4	F	000h	Reserved
	3-0	F	Varies	Device nominal form factor; 3h = 2.5", 4h = 1.8"
169	–	–	–	DATA SET MANAGEMENT command is supported
	15–1	F	000000000000000b	Reserved
	0	F	1b	1 = The trim bit in the DATA SET MANAGEMENT command is supported
170	–	F	0000h 0000h 0000h 0000h	Additional product identifier
174	–	F	0000h 0000h	Reserved
176	–	(O)V	Varies	Current media serial number (60 ASCII characters)

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
206	–	–	–	SCT command transport
	15–12	X	0000b	Vendor-specific
	11–6	F	000000b	Reserved
	5	F	1b	SCT command transport data tables are supported
	4	F	1b	SCT command transport features control is supported
	3	F	0b	SCT command transport error recovery control is supported
	2	F	1b	SCT command transport write same is supported
	1	F	0b	SCT command transport long sector access is supported
	0	F	1b	SCT command transport is supported
207	–	( )F	0000h 0000h	Reserved for CE-ATA
209	–	(O)	–	Alignment of logical blocks within a larger physical block
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–0	F	00000000000000b	Logical sector offset within the first physical sector where the first logical sector is placed
210	–	(O)V	0000h 0000h	Write-read-verify sector count mode 3 only
212	–	(O)F	0000h 0001h	Verify sector count mode 2 only
214	–	(O)	–	NV cache capabilities
	15–12	F	0000b	NV cache feature set version
	11–8	F	0000b	NV cache power mode feature set version
	7–5	F	000b	Reserved
	4	V	0b	1 = NV cache feature set is enabled
	3–2	F	00b	Reserved
	1	V	0b	1 = NV cache power mode feature set is enabled
	0	F	0b	1 = NV cache power mode feature set is supported
215	–	(O)V	0000h	NV cache size in logical blocks (LSW)
216	–	(O)V	0000h	NV cache size in logical blocks (MSW)
217	–	(M)F	0001h	Nominal media rotation rate (ATA8-ACS 1699-D revision 6)
	–	–	–	NV cache read transfer speed in MB/s (ATA8-ACS 1699-D revision 3f)
218	–	(O)V	0000h	NV cache write transfer speed in MB/s
219	–	–	–	NV cache options
	15–8	F	00h	Reserved
	7–0	F	00h	Device estimated time to spin-up in seconds
220	15–8	F	00h	Reserved
	7–0	V	00h	Write-read-verify feature set current mode
221	–	–	0000h	Reserved

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Table 5: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
222	–	–	–	Transport major revision number. 0000h or FFFFh = Device does not report version
	15–12	–	0001b	Transport type - 0 = Parallel, 1 = Serial, 2–15 = Reserved Parallel (type = 0), serial (type = 1)
	11–7	–	000000b	Reserved
	6	–	1b	1 = SATA rev 3.1 is supported
	5	–	1b	Reserved SATA rev 3.0
	4	–	1b	Reserved SATA rev 2.6
	3	–	1b	Reserved SATA rev 2.5
	2	–	1b	Reserved SATA II: Extensions
	1	–	1b	Reserved SATA 1.0a
	0	–	1b	ATA8-APT ATA8-AST
223	–	(M)F	0000h	Transport minor revision number
224	–	( )F	0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved for CE-ATA
234	–	(O)F	0001h	Minimum number of 512-byte units per DOWNLOAD MICRO-CODE command for mode 3
235	–	–	00FFh	Maximum number of 512-byte units per DOWNLOAD MICRO-CODE command for mode 3
236	–	–	0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved
243	–	–	0000h	Bit 14 = 1; supports FDE security features
244	–	–	0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	
255	–	(M)F	–	Integrity word
	15–8	–	Varies	Checksum
	7–0	–	A5h	Signature

Note: 1. F = The content of the word is fixed and does not change.
V = The content of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = The content of the word may be fixed or variable.
R = The content of the word is reserved and will be zero.
M = Support of the word is mandatory.
O = Support of the word is optional.

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Commands

Table 6: Supported ATA Command Set

See ATA-8 standard for command details

Command Name	Command Code (hex)
CHECK POWER MODE	98h or E5h
DATA SET MANAGEMENT	06h
DEVICE CONFIGURATION RESTORE	B1h/C0h
DEVICE CONFIGURATION FREEZE LOCK	B1h/C1h
DEVICE CONFIGURATION IDENTIFY	B1h/C2h
DEVICE CONFIGURATION SET	B1h/C3h
DOWNLOAD MICROCODE	92h
EXECUTE DEVICE DIAGNOSTIC	90h
FLUSH CACHE	E7h
FLUSH CACHE EXT	EAh
IDENTIFY DEVICE	ECh
IDLE	E3h or 97h
IDLE IMMEDIATE	E1h or 95h
INITIALIZE DEVICE PARAMETERS	91h
NOP	00h
READ BUFFER	E4h
READ DMA (with retry)	C8h
READ DMA (without retry)	C9h
READ DMA EXT	25h
READ FPDMA QUEUED	60h
READ LOG EXT	2Fh
READ LOG DMA EXT	47h
READ MULTIPLE	C4h
READ MULTIPLE EXT	29h
READ NATIVE MAX ADDRESS	F8h
READ NATIVE MAX ADDRESS EXT	27h
READ SECTOR(S) EXT	24h
READ SECTOR(S) (with retry)	20h
READ SECTOR(S) (without retry)	21h
READ VERIFY SECTOR EXT	42h
READ VERIFY SECTOR(S) (with retry)	40h
REQUEST SENSE DATA EXT	0Bh
SANITIZE DEVICE	B4h
SECURITY DISABLE PASSWORD	F6h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h

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Table 6: Supported ATA Command Set (Continued)

See ATA-8 standard for command details

Command Name	Command Code (hex)
SECURITY FREEZE LOCK	F5h
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SEEK	70h
SET FEATURES	EFh
SET MAX ADDRESS	F9h
SET MAX ADDRESS EXT	37h
SET MULTIPLE MODE	C6h
SLEEP	E6h or 99h
SMART DISABLE OPERATIONS	B0h/D9h
SMART ENABLE OPERATIONS	B0h/D8h
SMART ENABLE/DISABLE AUTOSAVE	B0h/D2h
SMART EXECUTE OFF-LINE IMMEDIATE	B0h/D4h
SMART READ DATA	B0h/D0h
SMART READ LOG	B0h/D5h
SMART RETURN STATUS	B0h/DAh
SMART WRITE LOG	B0h/D6h
STANDBY	E2h or 96h
STANDBY IMMEDIATE	E0h or 94h
WRITE BUFFER	E8h
WRITE DMA (with retry)	CAh
WRITE DMA (without retry)	CBh
WRITE DMA EXT	35h
WRITE DMA FUA EXT	3Dh
WRITE FPDMA QUEUED	61h
WRITE LOG EXT	3Fh
WRITE LOG DMA EXT	57h
WRITE MULTIPLE	C5h
WRITE MULTIPLE EXT	39h
WRITE MULTIPLE FUA EXT	CEh
WRITE SECTOR(S) (with retry)	30h
WRITE SECTOR(S) EXT	34h
WRITE UNCORRECTABLE EXT	45h

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Performance

Measured performance can vary for a number of reasons. The major factors affecting drive performance are the density of the drive and the interface of the host. Additionally, overall system performance can affect the measured drive performance. When comparing drives, it is recommended that all system variables are the same, and only the drive being tested varies.

Performance numbers will vary depending on the host system configuration.

Table 7: Drive Performance

Density	120GB	240GB	480GB	800GB	Unit
Sequential read (128KB transfer)	425	425	425	425	MB/s
Sequential write (128KB transfer)	200	330	375	375	MB/s
Random read (4KB transfer)	63,000	63,000	63,000	65,000	IOPS
Random write (4KB transfer)	23,000	33,000	35,000	24,000	IOPS
READ latency (TYP)	0.50	0.50	0.50	0.50	ms
WRITE latency (TYP)	1.5	1.5	1.5	1.5	ms

Notes:
1. Typical I/O performance numbers as measured using Iometer with a queue depth of 32 and write cache disabled.
2. Iometer measurements are performed in the steady state region.
3. 4KB transfers used for READ/WRITE latency values.
4. System variations may affect measured results.

Reliability

Micron's SSDs incorporate advanced technology for defect and error management. They use various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 8: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{16} bits	READ

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Mean Time to Failure

Mean time to failure (MTTF) for the SSD can be predicted based on the component reliability data using the methods referenced in the Telcordia SR-332 reliability prediction procedures for electronic equipment.

Table 9: MTTF

Density	MTTF (Operating Hours)[1]
120GB	2 million
240GB	2 million
480GB	2 million
800GB	2 million

Note: 1. The product achieves a MTTF of 2 million hours based on population statistics not relevant to individual units.

Endurance

Endurance for the SSD can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear-leveling efficiency of the drive. Total bytes written measured with 55°C case temperature within the total bytes written values listed in this document. The table below shows the drive lifetime for each SSD density based on predefined usage conditions.

Table 10: Drive Lifetime

Density	Drive Lifetime (Total Bytes Written)
120GB	0.5PB
240GB	1.0PB
480GB	1.9PB
800GB	1.9PB

Note: 1. Total bytes written were calculated assuming drive is 100% full (user capacity) and a workload of 100% random, aligned 4KB writes.

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Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: SATA Power Consumption

Density	Idle Average	Sequential Write Max (128KB transfer)	Sequential Read Max (128KB transfer)
120GB	1.2W	4W	<4W
240GB	1.2W	5W	<5W
480GB	1.2W	6W	<6W
800GB	1.2W	6.3W	<6.3W

Notes:
1. Data taken at 25°C using a 6 Gb/s SATA interface.
2. Sequential power measured during Iometer with 128KB transfer, RMS average over a 500ms window.

Table 12: Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Voltage input	V5	4.5	5.5	V
Operating temperature	T_C	0	70	°C
Non-operating temperature	–	–40	85	°C
Rate of temperature change	–	–	20	°C/hour
Relative humidity (non-condensing)	–	5	95	%

Table 13: Shock and Vibration

Parameter/Condition	Specification
Operating shock	1500G/0.5ms
Operating vibration	10–500Hz at 3.1G

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Compliance

Micron SSDs comply with the following:

- RoHS
- CE (Europe): EN55022, 2006 + A1:2007 and EN55024, 1998 + A1:2001 + A2:2003
- FCC: CFR Title 47, Part 15 Class A
- UL/cUL: approval to UL-60950-1, 2nd Edition, IEC 60950-1:2005 (2nd Edition); Am 1:2009, EN 60950-1 (2006) + A11:2009+ A1:2010 + A12:2011
- BSMI (Taiwan): approval to CNS 13438
- C-TICK (Australia, New Zealand): approval to AS/NZS CISPR22
- KCC RRL (Korea): approval to KCC-REM-MU2-P400m25
- W.E.E.E.: Compliance with EU WEEE directive 2002/96/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced
- TUV (Germany): approval to IEC60950/EN60950
- V_{CCI}
- IC (Canada):
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

FCC Rules

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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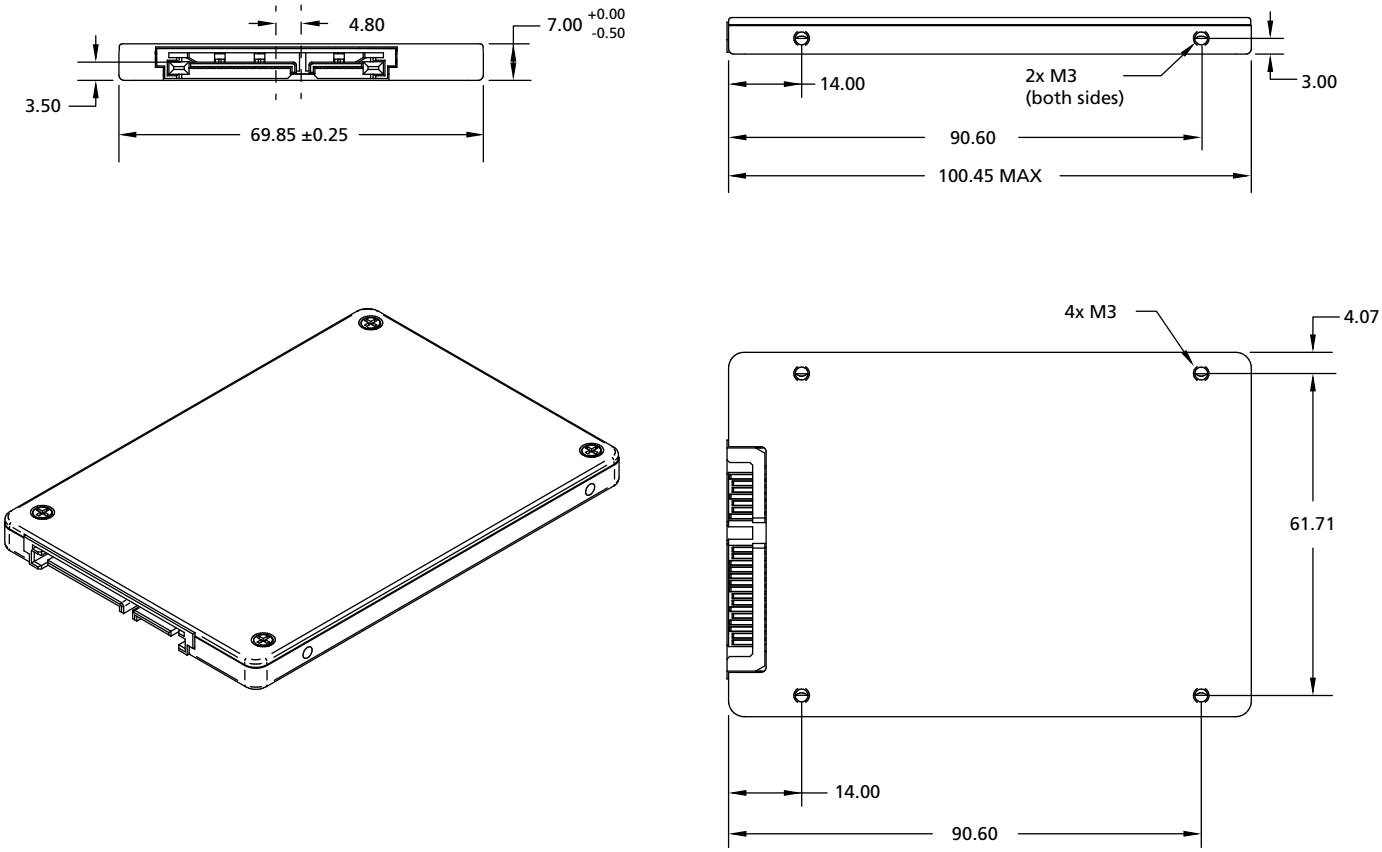
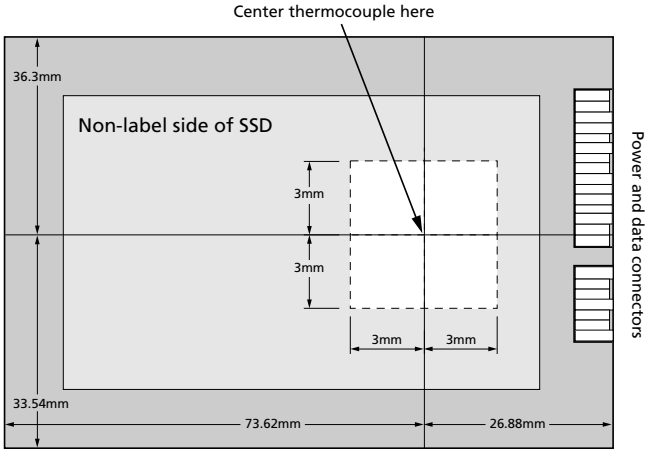
Package Dimensions

Figure 4: 2.5-Inch Package – 7mm



Note: 1. All dimensions are in millimeters per SFF-8201 REV 2.7.

Figure 5: Thermocouple Placement Guidelines for Temperature Measurement



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References

- Serial ATA: High-speed serialized AT attachment, Serial ATA working group, available at www.sata-io.org
- SATA 3.1 GOLD
- ATA-8 Rev. 4
- SFF-8201 Rev. 2.7

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Revision History

Rev. G – 02/15

- Updated Feature and Reference with SFF-8201 Rev. 2.7
- Updated Package Dimensions

Rev. F – 10/14

- Updated and added Reliability parameters in Feature
- Updated Table 8: Uncorrectable Bit Error Rate in Reliability

Rev. E – 8/14

- Updated device ID values
- Updated Idle Average values in Table 11: SATA Power Consumption

Rev. D – 4/14

- Status changed to Production
- Updated Table 5: Identify Device
- Updated note 2 in Table 11: SATA Power Consumption
- Revised operating vibration specification

Rev. C – 3/14

- Updated part numbers
- Revised performance specifications
- Updated device ID values

Rev. B – 11/13

- Revised performance specifications

Rev. A – 8/13

- Initial release

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